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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,960	11/10/2003	David S. Collins	BUR920030056US1	2959

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MCGUIRE WOODS LLP
1750 TYSONS BLVD.
SUITE 1800
MCLEAN, VA 22102-4215

EXAMINER
DINH, PAUL

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,960	COLLINS ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *22-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) None

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/03*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

This is a response to the election filed on 12/6/05.

Claims 1-21 = elected.

Claims 22-31 = withdrawn.

Claim Objections

Claim 19 is objected to because "the higher level circuit element (on line 4) lacks antecedent basis.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 is rejected because the "non-growable segments" finds no clear support in the specification.

Claims 2-21 are rejected because they depend from on claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –
(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-18 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art of record from IDS (11/14/03): Sue E. Strang, et al., "A design system for Auto Generation of ESD Circuits" International Cadence Usergroup, September 16-18, 2002, San Jose, CA (The office receives a total of 9 pages including cover page as page 1)

(Claim 1)

A user interface (ESD design systems, ESD CAD, Cadence design system in pages 1-2) for inputting a plurality of design parameters of a circuit;

An ESD kit comprising parameterized cells (p-cells) of low-level electronic components and p-cells of higher-level electronic circuit components (fig 2, 4-6, 9-13, tables 1-2), the higher-level electronic circuit components comprising growable and non-growable segments (see fixed, grow, growable, variable/change in (physical) size, adjust size and number of elements, diode string and clamp size be increases in size, i.e., pages 1, 4-8); and

A circuit schematic module creating ESD elements (fig 2-4, 11) for connection with the circuit based on the plurality of design parameters and using at least one of the low level electronic circuit components and higher level electronic circuit components.

(Claim 2) wherein the circuit schematic module places the ESD elements in the circuit (fig 2-4, 11)

(Claim 3) wherein said low level electronic components and higher-level electronic circuit components are in a hierarchical format (fig 2, 7-11, 13, table 2)

(Claim 4) wherein the higher level electronic circuit components form repetition groups of an underlying p-cell element to accommodate different inputted design parameters when forming the ESD elements (pages 7-8, fig 8, 10, 12)

(Claim 5) wherein the p-cells of lower order electronic components fix some variables and pass some variables to the higher order p-cell electronic components through inheritance (page 3)

(Claim 6) further comprising a translation module for translating schematic representations of the ESD elements to graphical representations of the ESD elements and translating the graphical representations of the ESD elements to the schematic representations of the ESD elements (fig 2-6, 8, 10-13)

(Claims 7-10) further comprising a library containing various types of the ESD elements (fig 2), a module for manipulating the ESD elements to conform with a design of the circuit (fig 2-4); a pointer (fig 3) to the various types of the ESD elements in the library; wherein the various types of the ESD elements are preset or user designed (page 3-4, fig 2-4).

(Claim 11) wherein the circuit schematic module creates one of a symbol and a schematic of the ESD elements (fig 4, 6, 8, 11-12)

(Claims 12-14) further comprising a graphical seed module for creating a graphical seed of at least the ESD elements and the circuit (page 2, 4-5, fig 5, 10); wherein the graphical seed module includes functions of **at least one of:** (i) Stretch, (ii) Conditional Inclusion, (iii) Repetition, (iv) Parameterized shapes, (v) Repeat along shape, (vi) Reference point, (vii) Inherited Parameters, (viii) Parameterized Layer, (ix) Parameterized Label, (x) Parameterized Property, (xi) Parameters, and (xii) Compile (page 2, 4-5, fig 5, 10); wherein the graphical seed module creates a graphical representation of the circuit and the designed ESD element for future fabrication (page 2, 4-5, fig 5, 10).

(Claim 15) wherein the circuit schematic module creates a boundary about the ESD elements containing circuit information and places the schematic within the circuit design (fig 2-4, pages 4-5).

(Claims 16-18) further comprising a module for providing modification of ESD interconnect parameterized cells based on information of the higher level electronic circuit components (fig 2-4); wherein said circuit schematic module provides a static p-cell substantiation translator box used for comparison of the ESD interconnect parameterized cell and robustness of the ESD kit (fig 2-4, 10-11); further comprising a component (fig 2) to identify and verify a connection of at least one of a circuit type, the ESD interconnect parameterized cell, ESD type and a pad.

(Claim 20) further comprising a component to establish an interconnection path of a pad level for an input pad and to verify an ESD interconnect at the pad level (page 3).

(Claim 21) wherein a p-cell is established which prevents a metal level to go below a given ESD width where a minimum width is established by conversion of a metal shape into the p-cell where the metal has an algorithm with a minimum function where the width never goes below a given width defined by a minimum ESD requirement (page 3).

Allowable Subject Matter

Claim 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 19 would be allowable because the prior art does not teach or suggest the limitation in claim 19.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner